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TITLE OF THE INVENTION

Multi-output DC-DC converter

BACKGROUND OF THE INVENTION

The present invention relates to a multi-output DC-DC converter, for use in a variety of electronic appliances, configured to receive a DC voltage from a battery or the like and to supply controlled DC voltages to a plurality of loads.

An apparatus having a circuit configuration shown in FIG. 8 has been used conventionally as a multi-output DC-DC converter. The input DC voltage E_i of a DC power supply 1 is input to the conventional multi-output DC-DC converter shown in FIG. 8. A main switch 3 formed of an N-MOSFET, an inductor 2, a diode 4 and a first output capacitor 5 are provided to constitute a boost converter (step-up converter). A first output voltage V_{o1} is output from the first output capacitor 5 to a first load 6. A control circuit 7 adjusts the ON/OFF period ratio of the main switch 3 to control the first output voltage V_{o1} . The first output voltage V_{o1} is stepped down by a series regulator 8 and output as a second output voltage V_{o2} from a second output capacitor 9 to a second load 10.

The operation of the boost converter shown in FIG. 8 will be described below briefly.

First, when the main switch 3 is ON, the input DC voltage E_i is applied to the inductor 2. At this time, a current flows through the inductor 2 and magnetic energy is stored. Next, when the main switch 3 becomes OFF, the magnetic energy stored in the inductor 2 is released via the diode 4 as a current for charging the first output capacitor 5. When it is assumed that the main switch 3 is turned ON/OFF in a constant cycle, the energy output via the inductor 2 in each cycle is higher as the ON period of the main switch 3 is longer, and the first output voltage V_{o1} is higher as the ON period of the main switch 3 is longer. In other words, the control circuit 7 controls the first output voltage V_{o1} by adjusting the ON/OFF period ratio of the main switch 3. On the other hand, the second output voltage V_{o2} obtained from the first output voltage V_{o1} is output via the series regulator 8.

In the conventional multi-output DC-DC converter configured as described above, a loss due to the series regulator 8 was caused, thereby lowering conversion efficiency. In addition, since the conventional multi-output DC-DC converter used a configuration comprising a plurality of switching converters, such as the above-mentioned boost converter, to obtain multiple outputs, the number of

components increased, whereby an apparatus incorporating such converters was made larger in size and higher in cost.

FIG. 9 is a circuit diagram showing a three-output boost converter configured to control a plurality of outputs by using less number of components (see Official Gazette of Japanese Examined Patent Publication No. Hei 7-40785, for example). Numerals assigned to components shown in FIG. 9 are the same as those shown in the drawings disclosed in the Official Gazette of Japanese Examined Patent Publication No. Hei 7-40785. By the application of an input V_{11} , magnetic energy is stored in an inductor L during a period while a switch S_1 makes contact with its contact A . The magnetic energy is released to each output during a period while the switch S_1 makes contact with its contact B . At that time, the magnetic energy is distributed to each output via a switch S_2 . The Official Gazette of Japanese Examined Patent Publication No. Hei 7-40785 discloses a method of controlling the period while the switch S_2 makes contact with each contact thereof so that all the output voltages are stabilized and of controlling the switch S_1 so that power is supplied to all loads just sufficiently.

An invention having a configuration based on

a technical concept similar to that of the Official Gazette of Japanese Examined Patent Publication No. Hei 7-40785 but adopting a different control method has also been proposed (see U.S. Patent No. 5,400,239, for example). U.S. Patent No. 5,400,239 discloses an insulating flyback converter having N outputs and being characterized in that N rectifying and smoothing circuits are connected to one output winding of a transformer via a switching transistor corresponding to the switch S2 of the boost converter shown in FIG. 9. In U.S. Patent No. 5,400,239, the switching frequency of a main switching transistor corresponding to the switch S1 is divided by N and allocated to the control of each output. In other words, the switching transistor corresponding to the switch S2 in U.S. Patent No. 5,400,239 is switched at $1/N$ of the switching frequency. The ON period of the main switching transistor corresponding to the switch S1 is adjusted in each switching cycle, whereby each output voltage is controlled.

A configuration wherein an inductor is commonly used for a plurality of boost converters is obtained by applying the conventional control method disclosed in U.S. Patent No. 5,400,239 to the conventional multi-output converter shown in FIG. 8. FIG. 10 is a circuit diagram of a boost converter

having two outputs, serving as a simple application example of this configuration. FIG. 11 is a diagram showing the waveforms of signals at the main sections of the configuration. The application example will be described below in detail.

In the boost converter having two outputs, shown in FIG. 10, an input DC voltage E_i is input from an input DC power supply 1. The boost converter comprises an inductor 2, a main switch 14, an auxiliary switch 15, a diode 11, a first output capacitor 5, a diode 12 connected in series with the auxiliary switch 15, a second output capacitor 9 and a control circuit 16. The main switch 14 and the auxiliary switch 15 are each formed of an N-MOSFET, for example. The control circuit 16 controls the main switch 14 and the auxiliary switch 15 so that they are driven in accordance with their respective predetermined ON and OFF periods.

In the boost converter having two outputs configured as described above and shown in FIG. 10, a first output voltage V_{o1} is output from the first output capacitor 5 to a first load 6, and a second output voltage V_{o2} is output from the second output capacitor 9 to a second load 10. The input/output conditions are represented by $V_{o1} > V_{o2} > E_i$. When the auxiliary switch 15 is OFF, the inductor 2, the

main switch 14, the diode 11 and the first output capacitor 5 constitute a boost converter. On the other hand, when the auxiliary switch 15 is ON, the inductor 2, the main switch 14, the diode 12 and the second output capacitor 9 constitute a boost converter.

In the control circuit 16, an output detection circuit 17 detects the first output voltage V_{o1} and the second output voltage V_{o2} . Furthermore, the output detection circuit 17 outputs error voltages V_{e1} and V_{e2} respectively obtained by amplifying the error between the detected output voltage V_{o1} and its desired value and by amplifying the error between the detected output voltage V_{o2} and its desired value. An oscillation circuit 18 outputs a sawtooth voltage V_t and a clock signal V_{t1} each having a predetermined cycle T . A PWM circuit 19 outputs a signal V_1 obtained as the result of the comparison between the error voltage V_{e1} and the sawtooth voltage V_t and also outputs a signal V_2 obtained as the result of the comparison between the error voltage V_{e2} and the sawtooth voltage V_t .

A frequency divider circuit 20 receives the signal V_{t1} and outputs a frequency-divided signal V_{t2} . A drive circuit 21 receives the signal V_1 , the signal V_2 and the frequency-divided signal V_{t2} and outputs a drive signal V_{g14} for the main switch 14 and a drive

signal Vg15 for the auxiliary switch 15. Furthermore, as the drive signal Vg14 from the drive circuit 21, the signal V1 is selected and output when the frequency-divided signal Vt2 is low, and the signal V2 is selected and output when the frequency-divided signal Vt2 is high.

FIG. 11 is a diagram showing the waveforms of the various signals in the boost converter having two outputs shown in FIG. 10 and the waveform of a current IL flowing through the inductor 2.

The operation of the conventional multi-output DC-DC converter during its normal operation will be described below by using FIGS. 10 and 11.

First, it is assumed that at time t0 in FIG. 11, the frequency-divided signal Vt2 is driven low by the clock signal Vt1 and the sawtooth voltage Vt starts rising. At this time, the frequency-divided signal Vt2, that is, the drive signal Vg15, is low, whereby the auxiliary switch 15 becomes OFF. On the other hand, the signal V1 obtained as the result of the comparison between the sawtooth voltage Vt and the error voltage Vel becomes high, and this signal is output as the drive signal Vg14. In other words, the main switch 14 becomes ON, the input DC voltage Ei is applied to the inductor 2, and magnetic energy is stored.

When the signal V_1 becomes low at time t_1 , the drive signal V_{g14} becomes low, and the main switch 14 becomes OFF. At this time, the magnetic energy stored in the inductor 2 is released as a current for charging the capacitor 5 via the diode 11 since the auxiliary switch 15 is OFF. This current decreases and becomes zero soon.

At time t_2 , the frequency-divided signal V_{t2} is driven high by the clock signal V_{t1} , and the sawtooth voltage V_t lowers abruptly and then starts rising again. At this time, the drive signal V_{g15} becomes high, and the auxiliary switch 15 becomes ON. On the other hand, the signal V_2 obtained as the result of the comparison between the sawtooth voltage V_t and the error voltage V_{e2} becomes high and is output as the drive signal V_{g14} . In other words, the main switch 14 becomes ON. At this time, the input DC voltage E_i is applied to the inductor 2, and magnetic energy is stored.

When the signal V_2 becomes low at time t_3 , the drive signal V_{g14} becomes low, and the main switch 14 becomes OFF. At this time, the magnetic energy stored in the inductor 2 is released as a current for charging the capacitor 9 via the diode 12 since the auxiliary switch 15 is ON. This current decreases and becomes zero soon.

At time t_4 , the drive signal V_{g15} becomes low, and the operation at time t_0 and thereafter is repeated.

The following equations (1) and (2) are established assuming that the inductance of the inductor 2 is L , that the ON period of the main switch 14 while the auxiliary switch 15 is OFF is T_{on1} , that the ON period of the main switch 14 while the auxiliary switch 15 is ON is T_{on2} , that the output current to the first load 6 is I_{o1} , and that the output current to the second load 10 is I_{o2} .

$$V_{o1} = E_i + \frac{(E_i \cdot T_{on1})^2}{4L \cdot T \cdot I_{o1}} \quad (1)$$

$$V_{o2} = E_i + \frac{(E_i \cdot T_{on2})^2}{4L \cdot T \cdot I_{o2}} \quad (2)$$

In the conventional boost converter having two outputs, configured as described above, the error voltages V_{e1} and V_{e2} change so that the first and second output voltages V_{o1} and V_{o2} are stabilized to their respective desired voltages, whereby the ON period of the main switch 14 is adjusted. In other words, the two boost converters wherein the main

switch 14 and the inductor 2 are commonly used are subjected to time-sharing control at half the oscillation frequency of the oscillation circuit 18. Hence, the first and second output voltages V_{o1} and V_{o2} are stabilized to their respective desired voltages.

As described above, the conventional multi-output DC-DC converter shown in FIG. 8 had a problem of causing a loss due to the series regulator and thereby having low conversion efficiency. In addition, since the conventional multi-output DC-DC converter shown in FIG. 8 used a configuration comprising a plurality of switching converters, such as boost converters, to obtain multiple outputs, the number of components increased, whereby an apparatus incorporating such converters was made larger in size and higher in cost.

On the other hand, in the configuration of the conventional multi-output DC-DC converter shown in FIG. 9, the number of components is decreased by commonly using the inductor, whereby a plurality of outputs can be controlled at high efficiency. In the configuration of the conventional multi-output DC-DC converter shown in FIG. 9, in the case of the control method disclosed in the Official Gazette of Japanese Examined Patent Publication No. Hei 7-40785, the

magnetic energy is stored in the inductor L during a period while the switch S1 makes contact with its contact A. This magnetic energy is distributed to each output by the switching operation of the switch S2 during a period while the switch S1 makes contact with its contact B. However, for example, in the case of the converter having three outputs shown in FIG. 9, when the above-mentioned control method is used, it is necessary to control four periods in one switching cycle of the switch S1. The four periods are a period while the switch S1 makes contact with its contact A, a period while the switch S1 makes contact with its contact B and the switch S2 distributes the magnetic energy to a first output, a period while the switch S1 makes contact with its contact B and the switch S2 distributes the magnetic energy to a second output, and a period while the switch S1 makes contact with its contact B and the switch S2 distributes the magnetic energy to a third output. A switching converter can be made smaller by raising its switching frequency. However, in the method of controlling the above-mentioned four periods, it was difficult to raise the switching frequency. Furthermore, there was a problem of causing switching losses and switching noise during the switching operation of the switch S2.

The above-mentioned problem of being

difficult to raise the switching frequency can be solved, just as in the case of the converter disclosed in U.S. Patent No. 5,400,239, more specifically, by applying the control method wherein the switching frequency is divided and assigned to the control of each output. This is described above by taking the boost converter having two outputs as an example and by using FIGS. 10 and 11. However, in the conventional converter configured as shown in FIG. 10, the current flowing through the inductor 2 did not become zero in some cases during the OFF period of the main switch 14. In a converter, the current flowing through the inductor 2 is desired to be zero during the OFF period of the main switch 14 because of the following reason.

For example, in the multi-output DC-DC converter shown in FIG. 10, in the case when the first output current I_{o1} is large and the current flowing through the diode 11 does not become zero during the OFF period of the main switch 14, the current I_L flowing through the inductor 2 has the waveform shown in FIG. 12. At this time, the output voltages V_{o1} and V_{o2} are represented by the following equations (3) and (4).

$$V_{o1} = \frac{T + T_{on1}}{T - T_{on1}} \cdot E_i - \frac{4L \cdot T \cdot I_{o1}}{(T - T_{on1})^2} \quad (3)$$

$$V_{o2} = E_i + \frac{\{(T + T_{on2}) \cdot E_i - (T - T_{on1}) \cdot V_{o1}\}^2}{4L \cdot T \cdot I_{o2}} \quad (4)$$

The first output voltage V_{o1} can be controlled by adjusting the ON period T_{on1} in accordance with the change of the output current I_{o1} . However, since the current flowing through the diode 11 does not become zero during the OFF period of the main switch 14, there is a restriction represented by $V_{o1} < E_i \cdot T / (T - T_{on1})$. Hence, even when $T_{on2} = 0$, the numerator of the second term in Equation (4) for obtaining the second output voltage V_{o2} has a value larger than zero. Therefore, in the case when the output current I_{o2} is small, the second output voltage V_{o2} rises and becomes uncontrollable. At the time of starting when the output has not risen sufficiently or when one of the outputs is overloaded and the voltage of the output lowers, the current flowing through the inductor 2 does not become zero during the OFF period of the main switch 14. In other words, the phenomenon shown in FIG. 12 occurs as a problem.

SUMMARY OF THE INVENTION

By dividing a switching frequency and by controlling a plurality of outputs, the present invention is intended to provide a highly reliable multi-output DC-DC converter comprising highly efficient switching converters configured so that the number of components is reduced by using an inductor in common, and preventing the output voltages from being raised by the magnetic energy remaining in the inductor and from becoming uncontrollable at the time of starting or overload.

In order to attain the above-mentioned object, the multi-output DC-DC converter in accordance with the present invention comprises first to n th (n : an integer of 2 or more) output circuits for receiving an input DC voltage and for outputting first to n th output DC voltages, a switching circuit, an inductor and a control circuit, wherein

the switching circuit has an ON state, in which the input DC voltage is applied to the inductor and magnetic energy is stored, and has first to n th OFF states, in which the magnetic energy is released to one of the first to n th output circuits,

the control circuit is configured to distribute the switching cycles of the switching circuit to first to n th outputs to be controlled and

to detect the first to nth output DC voltages, and further configured, in the case when one switching cycle of the switching circuit is used to control a kth ($1 \leq k \leq n$) output, to select a kth OFF state after the period of the ON state is adjusted so that the kth output DC voltage becomes a predetermined value and to maintain the kth OFF state until the release of the magnetic energy stored in the inductor to the kth output circuit is completed. By dividing the switching frequency and by controlling the plurality of outputs, the multi-output DC-DC converter in accordance with the present invention configured as described above can comprise highly efficient switching converters configured so that the number of components is reduced by using the inductor in common. Furthermore, the multi-output DC-DC converter prevents the output voltages from being raised by the magnetic energy remaining in the inductor and from becoming uncontrollable at the time of starting or overload. Still further, the multi-output DC-DC converter in accordance with the present invention is configured so that the operation shifts to the next cycle after the current flowing through the inductor becomes zero within one switching cycle. Hence, it is possible to avoid an overvoltage condition due to the occurrence that the current flowing through the inductor does not

become zero within one switching cycle.

The multi-output DC-DC converter in accordance with the present invention, may be configured so that the control circuit is configured to shift the k th OFF state to the ON state after the release of the magnetic energy stored in the inductor to the k th output circuit is completed.

Further, the multi-output DC-DC converter in accordance with the present invention may be configured so that the switching cycle of the switching circuit or the period from the first to n th OFF state is not smaller than a predetermined value.

The multi-output DC-DC converter in accordance with another aspect of the present invention comprises first to n th (n : an integer of 2 or more) output circuits for receiving an input DC voltage and for outputting first to n th output DC voltages, a switching circuit, an inductor and a control circuit, wherein

the switching circuit has an ON state, in which the input DC voltage is applied to the inductor and magnetic energy is stored, and has first to n th OFF states, in which the magnetic energy is released to one of the first to n th output circuits,

the control circuit is configured to distribute the switching cycles of the switching

circuit to first to nth outputs to be controlled and to detect the first to nth output DC voltages, and further configured, in the case when one switching cycle of the switching circuit is used to control a kth ($1 \leq k \leq n$) output, to select a kth OFF state after the period of the ON state is adjusted so that the kth output DC voltage becomes a predetermined value and to select an OFF state other than the kth OFF state when the kth output DC voltage exceeds a predetermined upper limit value. By dividing the switching frequency and by controlling the plurality of outputs, the multi-output DC-DC converter in accordance with the present invention configured as described above can comprise highly efficient switching converters configured so that the number of components is reduced by using the inductor in common. Furthermore, the multi-output DC-DC converter prevents the output voltages from being raised by the magnetic energy remaining in the inductor and from becoming uncontrollable at the time of starting or overload. Still further, in the multi-output DC-DC converter in accordance with the present invention, since the switching cycle is fixed, the current flowing through the inductor does not become zero within one switching cycle in some cases. However, the resulting overvoltage condition is detected, and the current is

released to the other output. Therefore, it is possible to avoid the overvoltage condition.

Furthermore, the multi-output DC-DC converter in accordance with the present invention may be configured so that the operation is stopped when all the 1st to nth output DC voltages exceed their upper limit values having been set respectively.

While the novel features of the invention are set forth particularly in the appended claims, the invention, both as to organization and content, will be better understood and appreciated, along with other objects and features thereof, from the following detailed description taken in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram showing the configuration of a multi-output DC-DC converter in accordance with Embodiment 1 of the present invention;

FIG. 2 is a waveform diagram showing the operation of the multi-output DC-DC converter in accordance with Embodiment 1 of the present invention;

FIG. 3 is a waveform diagram showing the operation of the multi-output DC-DC converter in accordance with Embodiment 1 of the present invention;

FIG. 4 is a circuit diagram showing the

configuration of a multi-output DC-DC converter in accordance with Embodiment 2 of the present invention;

FIG. 5 is a waveform diagram showing the operation of the multi-output DC-DC converter in accordance with Embodiment 2 of the present invention;

FIG. 6 is a circuit diagram showing the configuration of a multi-output DC-DC converter in accordance with Embodiment 3 of the present invention;

FIG. 7A is a waveform diagram showing the normal operation of the multi-output DC-DC converter in accordance with Embodiment 3 of the present invention;

FIG. 7B is a diagram showing the state of various signals in an overvoltage condition of the multi-output DC-DC converter in accordance with Embodiment 3 of the present invention;

FIG. 8 is the circuit diagram showing the configuration of the conventional multi-output DC-DC converter;

FIG. 9 is the circuit diagram showing the configuration of the conventional multi-output DC-DC converter;

FIG. 10 is the circuit diagram showing the configuration of the conventional multi-output DC-DC converter;

FIG. 11 is the waveform diagram showing the

operation of the conventional multi-output DC-DC converter; and

FIG. 12 is the waveform diagram showing the output current of the conventional multi-output DC-DC converter.

It will be recognized that some or all of the Figures are schematic representations for purposes of illustration and do not necessarily depict the actual relative sizes or locations of the elements shown.

DETAILED DESCRIPTION OF THE INVENTION

Preferred embodiments of a multi-output DC-DC converter in accordance with the present invention will be described below referring to the accompanying drawings.

«Embodiment 1»

FIG. 1 is a circuit diagram showing the configuration of a multi-output DC-DC converter in accordance with Embodiment 1 of the present invention. As shown in FIG. 1, in the multi-output DC-DC converter in accordance with Embodiment 1 of the present invention, an input DC voltage E_i is input from an input DC power supply 1. The multi-output DC-DC converter comprises an inductor 2, a switching

circuit 30, a diode 41, a diode 42, a first output capacitor 51, a second output capacitor 52 and a control circuit 80.

The switching circuit 30 comprises a main switch 31 and an auxiliary switch 32. Each of the switches is formed of an N-MOSFET, for example. The diode 42 is connected in series with the auxiliary switch 32. The control circuit 80 controls the main switch 31 and the auxiliary switch 32 so that they are driven in accordance with their respective predetermined ON and OFF periods.

In the multi-output DC-DC converter in accordance with Embodiment 1, a first output voltage V_{o1} is output from the first output capacitor 51 to a first load 6, and a second output voltage V_{o2} is output from the second output capacitor 52 to a second load 10. The input/output conditions are represented by $V_{o1} > V_{o2} > E_i$.

The ON state of the switching circuit 30 comprising the main switch 31 and the auxiliary switch 32 is a state wherein the main switch 31 is ON and the input DC voltage E_i is applied to the inductor 2. At this time, the ON/OFF state of the auxiliary switch 32 is not considered. The first OFF state of the switching circuit 30 is a state wherein the main switch 31 is OFF and the auxiliary switch 32 is OFF.

In the case when the auxiliary switch 32 is OFF as described above, the inductor 2, the main switch 31, the diode 41 and the capacitor 51 constitute a boost converter (step-up converter). The second OFF state of the switching circuit 30 is a state wherein the main switch 31 is OFF and the auxiliary switch 32 is ON. In the case when the auxiliary switch 32 is ON as described above, the inductor 2, the main switch 31, the diode 42 and the capacitor 52 constitute a boost converter (step-up converter).

As shown in FIG. 1, the control circuit 80 in accordance with Embodiment 1 comprises an output detection circuit 81, an oscillation circuit 82, a pulse width modulation circuit (hereafter referred to as a PWM circuit) 83, a frequency divider circuit 84 and a drive circuit 85.

The output detection circuit 81 of the control circuit 80 comprises resistors 811 and 812 for detecting the first output voltage V_{o1} , resistors 813 and 814 for detecting the second output voltage V_{o2} , a reference voltage source 815, an error amplifier 816 for amplifying the error between the detection voltage of the first output voltage V_{o1} and the voltage of the reference voltage source 815, and an error amplifier 817 for amplifying the error between the detection voltage of the second output voltage V_{o2} and the

voltage of the reference voltage source 815. The output detection circuit 81 outputs an error voltage V_{e1} from the error amplifier 816 and outputs an error voltage V_{e2} from the error amplifier 817.

The oscillation circuit 82 of the control circuit 80 comprises an oscillation capacitor 820 for outputting an oscillation voltage V_t , a constant-current source 821 for charging the oscillation capacitor 820, a voltage source 822 for outputting a voltage E_1 , a transistor 823 connected between the oscillation capacitor 820 and the voltage source 822, a voltage source 824 for outputting an voltage E_2 , a comparator 825 for comparing the oscillation voltage V_t with the voltage E_2 , a comparator 826 to which the voltage V_L across the inductor 2 is input, an AND gate 827 to which the output of the comparator 825 and the output of the comparator 826 are input, and an AND gate 829 to which the output of the AND gate 827 and the output of an inverter 828, the inversion of the output of the AND gate 827, are input. When the output of the AND gate 827 becomes high, the AND gate 829 outputs a one-shot pulse signal serving as a clock signal V_{t1} . The clock signal V_{t1} turns ON the transistor 823 for a short time, whereby the oscillation capacitor 820 is short-circuited and discharged to the voltage E_1 . When the transistor 823

is turned OFF, the oscillation capacitor 820 is charged by the constant current of the constant-current source 821. The clock signal V_{t1} is generated when the oscillation capacitor 820 is charged to the voltage E_2 or higher and when the voltage V_L of the inductor 2 is zero or lower. The comparator 825 has a hysteresis characteristic. It is thus assumed that after the oscillation voltage V_t has risen to the voltage E_2 or higher and the output of the comparator 825 has become high, the output of the comparator 825 does not become low unless the oscillation voltage V_t becomes lower than the voltage E_2 . In other words, the oscillation voltage V_t abruptly lowers to the voltage E_1 when the clock signal V_{t1} is generated and then rises linearly, thereby having a sawtooth waveform.

The PWM circuit 83 of the control circuit 80 comprises a comparator 831 for comparing the error voltage V_{e1} with the oscillation voltage V_t and for outputting a signal V_1 , and a comparator 832 for comparing the error voltage V_{e2} with the oscillation voltage V_t and for outputting a signal V_2 . The signal V_1 becomes high when the oscillation voltage V_t is not higher than the error voltage V_{e1} , and the signal V_2 becomes high when the oscillation voltage V_t is not higher than the error voltage V_{e2} .

The frequency divider circuit 84 of the control circuit 80 receives the clock signal V_{t1} and outputs a frequency-divided signal V_{t2} . The drive circuit 85 comprises an AND gate 851 to which the signal V_1 and the frequency-divided signal V_{t2} are input, an AND gate 852 to which the signal V_2 and the inverted signal of the frequency-divided signal V_{t2} are input, and an OR gate 853 to which the output of the AND gate 851 and the output of the AND gate 852 are input. The OR gate 853 outputs a drive signal V_{g31} for the main switch 31. The frequency-divided signal V_{t2} is output as a drive signal V_{g32} for the auxiliary switch 32. Hence, when the frequency-divided signal V_{t2} is low, the signal V_1 is selected and output as the drive signal V_{g31} . When the frequency-divided signal V_{t2} is high, the signal V_2 is selected and output as the drive signal V_{g31} .

FIG. 2 is a diagram showing the waveforms of the various signals generated in the control circuit 80, the current I_L flowing through the inductor 2 and the voltage V_L across the inductor 2, in Embodiment 1 configured as described above.

The operation of the multi-output DC-DC converter in accordance with Embodiment 1 of the present invention will be described below by using FIGS. 1 and 2.

First, it is assumed that at time t_0 in FIG. 2, the frequency-divided signal V_{t2} , that is, the drive signal V_{g32} , is driven low by the clock signal V_{t1} , whereby the auxiliary switch 32 becomes OFF and the oscillation voltage V_t starts rising. The signal V_1 obtained as the result of the comparison between the oscillation voltage V_t and the error voltage V_{e1} is selected as the drive signal V_{g31} . Since the drive signal V_{g31} is high, the main switch 31 becomes ON (the switching circuit 30 becomes ON), whereby the input DC voltage E_i is applied to the inductor 2 and magnetic energy is stored.

When the rising oscillation voltage V_t and the error voltage V_{e1} intersect with each other at time t_1 , the signal V_1 and the drive signal V_{g31} become low, whereby the main switch 31 becomes OFF. At this time, the magnetic energy stored in the inductor 2 is released as a current for charging the capacitor 51 via the diode 41 since the auxiliary switch 15 is OFF (the switching circuit 30 is in its first OFF state). At this time, the voltage ($V_{o1} - E_i$), that is, the difference between the first output voltage V_{o1} and the input DC voltage E_i , is applied as the voltage V_L of the inductor 2 in the case when the forward voltage drop of the diode 41 is neglected. Then, the oscillation voltage V_t rises continuously,

exceeds the voltage E_2 and stops rising soon since the constant-current source 821 is saturated.

On the other hand, the current I_L of the inductor 2 decreases and becomes zero soon at time t_2 . At this time, the voltage V_L of the inductor 2 starts free oscillation and lowers from the voltage $(V_{o1} - E_i)$.

When the voltage V_L of the inductor 2 becomes zero at time t_3 , the clock signal V_{t1} is generated, and the frequency-divided signal V_{t2} becomes high, whereby the oscillation voltage V_t lowers abruptly to the voltage E_1 and then starts rising again. At this time, the drive signal V_{g32} also becomes high, and the auxiliary switch 32 becomes ON. On the other hand, the signal V_2 obtained as the result of the comparison between the oscillation voltage V_t and the error voltage V_{e2} becomes high. This signal is selected and output as the drive signal V_{g31} . Hence, the main switch 31 becomes ON (the switching circuit 30 becomes ON), whereby the input DC voltage E_i is applied to the inductor 2 and magnetic energy is stored.

When the rising oscillation voltage V_t and the error voltage V_{e2} intersect with each other at time t_4 , the signal V_2 and the drive signal V_{g31} become low, whereby the main switch 31 becomes OFF.

At this time, the magnetic energy stored in the inductor 2 is released as a current for charging the capacitor 52 via the diode 42 since the auxiliary switch 32 is ON (the switching circuit 30 is in its second OFF state). At this time, the voltage ($V_{o2} - E_i$), that is, the difference between the second output voltage V_{o2} and the input DC voltage E_i , is applied as the voltage V_L of the inductor 2 in the case when the forward voltage drop of the diode 42 is neglected. Then, the oscillation voltage V_t rises continuously and exceeds the voltage E_2 .

On the other hand, the current I_L of the inductor 2 decreases and becomes zero soon at time t_5 . At this time, the voltage V_L of the inductor 2 starts free oscillation and lowers from the voltage ($V_{o2} - E_i$). The voltage V_L decreases and becomes zero soon.

When the voltage V_L of the inductor 2 becomes zero at time t_6 , the clock signal V_{t1} is generated, and the frequency-divided signal V_{t2} becomes low, whereby the oscillation voltage V_t lowers abruptly to the voltage E_1 and then starts rising again. In other words, after time t_6 , the operation at time t_0 and thereafter is repeated.

It is assumed that the inductance of the inductor 2 is L , that the ON period of the main switch 31 while the auxiliary switch 32 is OFF is T_{on1} , that

the OFF period of the main switch 31 while the auxiliary switch 32 is OFF is T_{off1} , that the ON period of the main switch 31 while the auxiliary switch 32 is ON is T_{on2} , and that the OFF period of the main switch 31 while the auxiliary switch 32 is ON is T_{off2} . In addition, it is assumed that the output current to the first load 6 is I_{o1} , and that the output current to the second load 10 is I_{o2} . Furthermore it is assumed that the forward voltage drops of the diodes 41 and 42 are neglected, and that transient periods between time t_2 and t_3 and between time t_5 and t_6 are neglected since these periods are shorter than the other periods. On the basis of these assumptions, the following equations (5) and (6) are established.

$$V_{o1} = E_i + \frac{T_{on1}}{T_{on1} + T_{on2}} \cdot \frac{E_i}{I_{o1}} \cdot \left(\frac{E_i \cdot T_{on1}}{2L} - I_{o1} - \frac{T_{on1}}{T_{on2}} \cdot I_{o2} \right) \quad (5)$$

$$V_{o2} = E_i + \frac{T_{on2}}{T_{on1} + T_{on2}} \cdot \frac{E_i}{I_{o2}} \cdot \left(\frac{E_i \cdot T_{on2}}{2L} - I_{o2} - \frac{T_{on2}}{T_{on1}} \cdot I_{o1} \right) \quad (6)$$

The error voltages V_{e1} and V_{e2} change so that the first and second output voltages V_{o1} and V_{o2}

are stabilized to their respective desired voltages, whereby the ON period of the main switch 31 is adjusted. In other words, in the multi-output DC-DC converter in accordance with Embodiment 1, the two boost converters wherein the main switch 31 and the inductor 2 are commonly used are subjected to time-sharing control. Hence, the first and second output voltages V_{o1} and V_{o2} are stabilized to their respective desired voltages.

In the multi-output DC-DC converter in accordance with Embodiment 1, the clock signal V_{t1} is generated only when the voltage V_L of the inductor 2 becomes zero or less. This indicates that the clock signal V_{t1} is generated after the magnetic energy stored in the inductor 2 is released as a current and lost. Hence, no magnetic energy remains in the inductor 2 even at the time of starting or overload. Therefore, output voltage rising to an uncontrollable level is securely avoided in the multi-output DC-DC converter in accordance with Embodiment 1.

In Embodiment 1, when the second load 10 is reduced for example, the second output current I_{o2} decreases. As the second output current I_{o2} decreases, the switching cycle assigned to the control of this output becomes shorter. FIG. 3 is a diagram showing the waveforms of the signals of the various sections

during operation at the time when the second load 10 is reduced. FIG. 3 also shows the waveforms of the outputs of the comparators 825 and 826 in addition to the waveforms of the signals of the various sections, shown in FIG. 2.

The operation at the time when the second load 10 is reduced will be described below by using FIGS. 1 and 3.

Since the operations of the various sections in the period from time t_0 to t_3 are the same as those shown in FIG. 2 described above, they are not described herein. When the rising oscillation voltage V_t and the error voltage V_{e2} intersect with each other at time t_4 , the main switch 31 becomes OFF. Hence, the magnetic energy stored in the inductor 2 is released as a current for charging the capacitor 52 via the diode 42.

On the other hand, the current of the inductor 2 decreases and becomes zero soon at time t_5 . When the current of the inductor 2 becomes zero, the voltage V_L across the inductor 2 starts free oscillation. This voltage V_L lowers from the voltage $(V_{o2} - E_i)$ and becomes zero soon, whereby the output of the comparator 826 becomes high. However, since the oscillation voltage V_t does not reach the voltage E_2 at this time, the output of the comparator 825 is

low, whereby the clock signal V_{t1} remains low. By the free oscillation of the voltage V_L , the output of the comparator 826 becomes high and low repeatedly.

At time t_6 , the oscillation voltage V_t reaches the voltage E_2 , and the output of the comparator 825 becomes high. When the output of the AND gate 826 becomes high after this, a one-shot pulse signal is generated as the clock signal V_{t1} . At time t_7 , the frequency-divided signal V_{t2} becomes low, whereby the oscillation voltage V_t lowers abruptly to the voltage E_1 and then starts rising again. In other words, after time t_7 , the operation at time t_0 and thereafter is repeated.

In the multi-output DC-DC converter in accordance with Embodiment 1 of the present invention, as the second output current I_{o2} decreases owing to the reduction of the load 10 , the switching cycle assigned to this output control becomes shorter. However, as described above, the multi-output DC-DC converter in accordance with Embodiment 1 is configured so that the clock signal V_{t1} for starting the next switching cycle is not generated while the oscillation capacitor 820 is charged from the voltage E_1 to the voltage E_2 . In other words, in the multi-output DC-DC converter in accordance with Embodiment 1, the switching cycle is set at a minimum period.

《Embodiment 2》

A multi-output DC-DC converter in accordance with Embodiment 2 of the present invention will be described below by using FIGS. 4 and 5.

FIG. 4 is a circuit diagram showing the configuration of the multi-output DC-DC converter in accordance with Embodiment 2 of the present invention. The input DC power supply 1, the inductor 2, the switching circuit 30 comprising the main switch 31 and the auxiliary switch 32, the diode 41, the first output capacitor 51, the diode 42 and the second output capacitor 52 described in the explanations of the above-mentioned Embodiment 1 are substantially the same as those of Embodiment 2 with respect to functions and configurations. Hence, they are designated by the same numerals, and their detailed explanations are omitted. The multi-output DC-DC converter in accordance with Embodiment 2 differs from the multi-output DC-DC converter in accordance with Embodiment 1 in the configuration and operation of a control circuit 90 for controlling the main switch 31 and the auxiliary switch 32 so that they are driven in accordance with their respective predetermined ON and OFF periods.

The output detection circuit 81, the PWM

circuit 83 and the frequency divider circuit 84 of the control circuit 90 are the same as those of the multi-output DC-DC converter in accordance with Embodiment 1 shown in FIG. 1 with respect to functions and configurations. Hence, they are designated by the same numerals, and their detailed explanations are omitted. The control circuit 90 differs from the control circuit 80 in accordance with Embodiment 1 in that an overvoltage protection circuit 91 is added and that an oscillation circuit 92 and a drive circuit 95 respectively differ from the oscillation circuit 82 and the drive circuit 85 of Embodiment 1 in configuration.

The overvoltage protection circuit 91 of the control circuit 90 comprises two resistors 911 and 912 for detecting the first output voltage V_{o1} , two resistors 913 and 914 for detecting the second output voltage V_{o2} , a voltage source 915, a comparator 916 for comparing the detection voltage of the first output voltage V_{o1} with the voltage of the voltage source 915, and a comparator 917 for comparing the detection voltage of the second output voltage V_{o2} with the voltage of the voltage source 915. A signal V_{x1} is output from one of the comparators, that is, the comparator 916, and a signal V_{x2} is output from the other comparator, that is, the comparator 917.

The overvoltage protection circuit 91 further comprises a NOR gate 918 to which the signals V_{x1} and V_{x2} are input, and a shutdown circuit 919 to which the output of this NOR gate 918 is input. When the first output voltage V_{o1} gets into an overvoltage condition, the signal V_{x1} becomes low. When the second output voltage V_{o2} gets into an overvoltage condition, the signal V_{x2} becomes low. Furthermore, when both the first output voltage V_{o1} and the second output voltage V_{o2} get into overvoltage conditions, the output of the NOR gate 918 becomes high, and the shutdown circuit 919 is operated. When the shutdown circuit 919 is operated, the control circuit 90 stops its operation. The operation is not resumed unless the input DC voltage E_i lowers sufficiently.

The oscillation circuit 92 has a signal source 920 for generating a clock signal V_{t1} having a predetermined cycle T . The oscillation circuit 92 is configured so that the oscillation capacitor 820 is charged by the constant current of the constant-current source 821 and discharged by a transistor 823 that is turned ON/OFF by the clock signal V_{t1} . The oscillation capacitor 820 having been charged is short-circuited by the transistor 823 and discharged to the voltage E_1 of a voltage source 822. In other words, the oscillation circuit 92 is configured so as

to output the clock signal V_{t1} and an oscillation voltage V_t having a sawtooth oscillation waveform synchronized with this clock signal V_{t1} .

The AND gate 851, the AND gate 852 and the OR gate 853 of the drive circuit 95 are the same as those of the drive circuit 85 of the control circuit 80 of the multi-output DC-DC converter in accordance with Embodiment 1 with respect to configuration. Hence, when the frequency-divided signal V_{t2} is low, the signal V_1 is selected and output as the drive signal V_{g31} . When the frequency-divided signal V_{t2} is high, the signal V_2 is selected and output as the drive signal V_{g31} . The selection and output carried out as described above are the same as those in the case of the multi-output DC-DC converter in accordance with Embodiment 1.

The drive circuit 95 in accordance with Embodiment 2 differs from the drive circuit 85 in accordance with Embodiment 1 as described below. The drive circuit 95 is additionally provided with an AND gate 951 to which the inverted signal of the signal V_{x1} and the signal V_{x2} are input, an AND gate 952 to which the signal V_{x2} and the signal V_{t2} are input, and an OR gate 953 to which the output of the AND gate 951 and the output of the AND gate 952 are input. Furthermore, in Embodiment 2, the output of the OR

gate 953 is output as the drive signal V_{g32} for the auxiliary switch 32.

The operation of the multi-output DC-DC converter in accordance with Embodiment 2 of the present invention will be described below.

First, the operation of the multi-output DC-DC converter during its normal operation wherein both the first output voltage V_{o1} and the second output voltage V_{o2} are not in overvoltage conditions will be described below. In the case of this normal operation, both the signals V_{x1} and V_{x2} are high. Hence, in the drive circuit 95, the output of the AND gate 951 is low, and the output of the AND gate 952 is the frequency-divided signal V_{t2} . The OR of these, serving as the drive signal V_{g32} , is the frequency-divided signal V_{t2} . Therefore, the operation of the control circuit 90 is similar to the operation of the control circuit 80 of the multi-output DC-DC converter in accordance with the above-mentioned Embodiment 1, except that the clock signal V_{t1} is set at a predetermined cycle T . In other words, the switching cycle during the normal operation of the multi-output DC-DC converter in accordance with Embodiment 2 is set at T . Except for this, the fundamental operations are similar to those of the multi-output DC-DC converter in accordance with the above-mentioned Embodiment 1.

Next, for example, the operation in the case when the first load 6 is increased and the first output current I_{o1} is in an overcurrent condition will be described below.

In this case, a phenomenon occurs wherein the current flowing through the inductor 2 does not become zero within the switching cycle assigned to the control of the first output voltage V_{o1} . The magnetic energy not released but remaining in the inductor 2 is released as a current for charging the capacitor 52 in the second OFF state in the next switching cycle. If the average value of this release current is larger than the current consumed by the second load 10, the second output voltage V_{o2} becomes uncontrollable and rises, whereby the second output voltage V_{o2} gets into an overvoltage condition.

When the second output voltage V_{o2} gets into the overvoltage condition, the comparator 917 is inverted, and the signal V_{x2} becomes low. On the other hand, the signal V_{x1} remains high at this time. In the drive circuit 95, both the outputs of the AND gate 951 and the AND gate 952 are low, whereby the OR of these, serving as the drive signal V_{g32} , is low. In other words, the auxiliary switch 32 becomes OFF (the first OFF state of the switching circuit 30) regardless of the state of the frequency-divided

signal V_{t2} . The current flowing through the inductor 2 is released to the circuit through which the first output current I_{o1} being in an overcurrent condition flows, whereby the overvoltage condition of the second output voltage V_{o2} is avoided.

Next, the operation in the case when the second load 10 is increased and the second output current I_{o2} is in an overcurrent condition will be described below.

In this case, a phenomenon occurs wherein the current flowing through the inductor 2 does not become zero within the switching cycle assigned to the control of the second output voltage V_{o2} . The magnetic energy not released but remaining in the inductor 2 is released as a current for charging the capacitor 51 in the first OFF state in the next switching cycle. If the average value of this release current is larger than the current consumed by the first load 6, the first output voltage V_{o1} becomes uncontrollable and rises, whereby the first output voltage V_{o1} gets into an overvoltage condition.

When the first output voltage V_{o1} gets into the overvoltage condition, the comparator 916 is inverted, and the signal V_{x1} becomes low. On the other hand, the signal V_{x2} remains high at this time. In the drive circuit 95, the output of the AND gate

951 is high, whereby the drive signal V_{g32} is also high. In other words, the auxiliary switch 32 becomes ON (the second OFF state of the switching circuit 30) regardless of the state of the frequency-divided signal V_{t2} . The current flowing through the inductor 2 is released to the circuit through which the second output current I_{o2} being in an overcurrent condition flows, whereby the overvoltage condition of the first output voltage V_{o1} is avoided.

FIG. 5 is a waveform diagram showing how the overvoltage condition of the first output voltage V_{o1} is avoided. Each time the first output voltage V_{o1} reaches its upper limit value at which the signal V_x becomes low, the switching circuit 30 is shifted from the first OFF state to the second OFF state. By this operation of the switching circuit 30, the first output voltage V_{o1} does not exceed the upper limit value, whereby its overvoltage condition is avoided.

As described above, in the multi-output DC-DC converter in accordance with Embodiment 2, even if the current flowing through the inductor 2 does not become zero within one switching cycle and an output voltage rises and becomes uncontrollable at the time of starting or overload, the overvoltage condition is detected, and the magnetic energy remaining in the inductor 2 is released to the other output. The

multi-output DC-DC converter in accordance with Embodiment 2 configured as described above can securely avoid the overvoltage condition at the time of starting or overload.

The problem wherein an output voltage rises and becomes uncontrollable may be caused by wire breakage in the output detection circuit 81 of the control circuit 90, for example. Therefore, as shown in FIG. 4, the output detection circuit 81 and the overvoltage protection circuit 91 are respectively provided with individual detection lines, although these circuits detect the same output voltages. Furthermore, in the above-mentioned uncontrollable condition owing to the abnormality in the control circuit 90, all the outputs get into overvoltage conditions, and the output of the NOR gate 918 of the overvoltage protection circuit 91 becomes high. Hence, the shutdown circuit 919 operates to stop the operation of the converter itself, thereby ensuring safety.

《Embodiment 3》

A multi-output DC-DC converter in accordance with Embodiment 3 of the present invention will be described below by using FIGS. 6, 7A and 7B.

FIG. 6 is a circuit diagram showing the

configuration of the multi-output DC-DC converter in accordance with Embodiment 3 of the present invention. A configuration having two step-up outputs is described in the explanations of the above-mentioned Embodiments 1 and 2. In the multi-output DC-DC converter in accordance with Embodiment 3, a configuration having two step-up outputs and one inverted output will be described below.

As shown in FIG. 6, in the multi-output DC-DC converter in accordance with Embodiment 3, an input DC voltage E_i is input from an input DC power supply 1. The multi-output DC-DC converter comprises an inductor 2, a switching circuit 30A, a diode 41, a diode 42, a diode 43, a first output capacitor 51, a second output capacitor 52, a third capacitor 53 and a control circuit 100. The switching circuit 30A comprises a first main switch 31, an auxiliary switch 32 and a second main switch 33. Each of the switches is formed of an N-MOSFET, for example. The control circuit 100 controls the main switch 31, the auxiliary switch 32 and the second main switch 33 so that they are driven in accordance with their respective predetermined ON and OFF periods. The diode 42 is connected in series with the auxiliary switch 32.

In the multi-output DC-DC converter in accordance with Embodiment 3, a first output voltage

Vo1 is output from the first output capacitor 51 to a first load 6. A second output voltage Vo2 is output from the second output capacitor 52 to a second load 10. A third output voltage Vo3 is output from the third output capacitor 53 to a third load 63. The input/output conditions are represented by $V_{o1} > V_{o2} > E_i > 0 > V_{o3}$.

The ON state of the switching circuit 30A is a state wherein both the first main switch 31 and the second main switch 33 are ON and the input DC voltage E_i is applied to the inductor 2. At this time, the ON/OFF state of the auxiliary switch 32 is not considered. The first OFF state of the switching circuit 30A is a state wherein the first main switch 31 is OFF, the second main switch 33 is ON and the auxiliary switch 32 is OFF. When the second main switch 33 is ON and the auxiliary switch 32 is OFF, the inductor 2, the first main switch 31, the diode 41 and the capacitor 51 constitute a boost converter. The second OFF state of the switching circuit 30A is a state wherein the first main switch 31 is OFF, the second main switch 33 is ON and the auxiliary switch 32 is ON. When the second main switch 33 is ON and the auxiliary switch 32 is ON, the inductor 2, the first main switch 31, the diode 41 and the capacitor 52 constitute a boost converter. The third OFF state

of the switching circuit 30A is a state wherein the first main switch 31 is ON and the second main switch 33 is OFF. At this time, the ON/OFF state of the auxiliary switch 32 is not considered. When the first main switch 31 is ON, the second main switch 33, the inductor 2, the diode 43 and the capacitor 53 constitute a buck-boost converter (inverted converter).

The output detection circuit 110 of the control circuit 100 shown in FIG. 6 detects the first output voltage V_{o1} , the second output voltage V_{o2} and the third output voltage V_{o3} . The error between each output voltage and its desired value is obtained. The respective errors are amplified, and error voltages V_{e1} , V_{e2} and V_{e3} are output. The output detection circuit 110 in accordance with Embodiment 3 differs from the output detection circuit 81 in accordance with the above-mentioned Embodiment 1 or Embodiment 2 only in that the number of inverted outputs is increased by one. The fundamental operation of the output detection circuit 110 is thus similar to that of the output detection circuit 81. Hence, the configuration of the output detection circuit 110 is not described in detail.

The PWM circuit 130 of the control circuit 100 outputs a signal V_1 obtained as the result of the comparison between the error voltage V_{e1} and the

sawtooth voltage V_t , a signal V_2 obtained as the result of the comparison between the error voltage V_{e2} and the sawtooth voltage V_t and a signal V_3 obtained as the result of the comparison between the error voltage V_{e3} and the sawtooth voltage V_t . The PWM circuit 130 in accordance with Embodiment 3 differs from the PWM circuit 83 in accordance with the above-mentioned Embodiment 1 or Embodiment 2 only in that a circuit for controlling an inverted output is additionally provided. The fundamental operation of the PWM circuit 130 is thus similar to that of the PWM circuit 83. Hence, the configuration of the PWM circuit 130 is not described in detail.

The overvoltage protection circuit 111 of the control circuit 100 has an overvoltage protection circuit 112. The overvoltage protection circuit 112 detects the first output voltage V_{o1} , the second output voltage V_{o2} and the third output voltage V_{o3} , and outputs signals V_{x1} , V_{x2} and V_{x3} , each of which is obtained as the result of the comparison between the absolute value of each of the output voltages and its maximum preset value. When the first output voltage V_{o1} gets into an overvoltage condition, the signal V_{x1} becomes low. When the second output voltage V_{o2} gets into an overvoltage condition, the signal V_{x2} becomes low. When the third output voltage V_{o3} gets into an

overvoltage condition, the signal V_{x3} becomes low. Furthermore, the overvoltage protection circuit 111 has a NOR gate 118 to which the signals V_{x1} , V_{x2} and V_{x3} are input. In the case when all the outputs get into overvoltage conditions, the output of the NOR gate 118 becomes high, thereby activating a shutdown circuit 119. In other words, when the first output voltage V_{o1} , the second output voltage V_{o2} and the third output voltage V_{o3} get into overvoltage conditions, the shutdown circuit 119 is activated. When the shutdown circuit 119 is activated, the operation of the control circuit 100 is stopped, and the operation is not resumed unless the input DC voltage E_i lowers sufficiently.

The oscillation circuit 92 of the control circuit 100 is the same as the oscillation circuit 92 shown in FIG. 4 in accordance with the above-mentioned Embodiment 2 with respect to configuration. The oscillation circuit 92 outputs the clock signal V_{t1} and the sawtooth voltage V_t having a predetermined cycle T .

Embodiment 3 is provided with two frequency divider circuits 84 and 140. The frequency divider circuit 84 receives the clock signal V_{t1} and outputs a frequency-divided signal V_{t2} . The frequency divider circuit 140 receives the frequency-divided signal V_{t2}

and outputs a frequency-divided signal Vt3.

The drive circuit 150 of the control circuit 100 comprises an AND gate 151 to which the frequency-divided signal Vt2 and the frequency-divided signal Vt3 are input, an AND gate 152 to which the output V32 of the AND gate 151 and the signal V2 are input, an AND gate 153 to which the frequency-divided signal Vt2 and the inverted signal of the frequency-divided signal Vt3 are input, an AND gate 154 to which the signal V1 and the inverted signal of the frequency-divided signal Vt2 are input, an OR gate 155 for outputting a signal V31 obtained as the OR of the outputs of the AND gate 152, the AND gate 153 and the AND gate 154, and an OR gate 156 for outputting a signal V33 obtained as the OR of the signal V3, the inverted signal of the frequency-divided signal Vt2 and the frequency-divided signal Vt3. Furthermore, the drive circuit 150 comprises a NOR gate 161 to which the signal Vx1 and the signal Vx2 are input, an OR gate 162 to which the output of the NOR gate 161 and the signal V31 are input, an AND gate 163 to which the output of the OR gate 162 and the signal Vx3 are input, an OR gate 164 to which the inverted signal of the signal Vx1 and the signal V32 are input, an AND gate 165 to which the output of the OR gate 164 and the signal Vx3 are input, an OR gate 166 to which the

signals V_{x1} and V_{x2} are input, an AND gate 167 to which the output of the OR gate 166 and the signal V_{33} are input, and an OR gate 168 to which the output of the AND gate 167 and the inverted signal of the signal V_{x3} are input. The AND gate 163 outputs a drive signal V_{g31} for the first main switch 31, the AND gate 165 outputs a drive signal V_{g32} for the auxiliary switch 32, and the OR gate 168 outputs a drive signal V_{g33} for the second main switch 33.

Since all the signals V_{x1} , V_{x2} and V_{x3} output from the overvoltage protection circuit 111 are high during the normal operation, the output of the NOR gate 161 is low, the OR gate 162 outputs the signal V_{31} , and the AND gate 163 outputs the signal V_{31} as the drive signal V_{g31} . In addition, the OR gate 164 outputs the signal V_{32} , and the AND gate 165 outputs the signal V_{32} as the drive signal V_{g32} . Furthermore, the output of the OR gate 166 is high, the AND gate 167 outputs the signal V_{33} , and the OR gate 168 outputs the signal V_{33} as the drive signal V_{g33} .

FIG. 7A is a diagram showing the waveforms of the various signals and the current I_L flowing through the inductor 2 during the normal operation of the multi-output DC-DC converter in accordance with Embodiment 3. The normal operation of the multi-

output DC-DC converter in accordance with Embodiment 3 of the present invention will be described below by using FIGS. 6, 7A and 7B.

First, it is assumed that at time t_0 in FIG. 7A, the frequency-divided signal V_{t2} is driven low by the clock signal V_{t1} but the frequency-divided signal V_{t3} remains low. At this time, since the output of the AND gate 151, that is, the signal V_{32} , is low, the drive signal V_{g32} becomes low, and the auxiliary switch 32 becomes OFF. Since both the outputs of the AND gates 152 and 153 are low, the signal V_1 output from the AND gate 154 is output as the signal V_{31} via the OR gate 155. In other words, the signal V_1 obtained as the result of the comparison between the oscillation voltage V_t and the error voltage V_{e1} is selected as the drive signal V_{g31} . Since the signal V_1 , that is, the drive signal V_{g31} , is high, the first main switch 31 becomes ON. In addition, since the output of the OR gate 156, that is, the signal V_{33} , is high, the drive signal V_{g33} also becomes high, and the second main switch 33 becomes ON. Since both the first main switch 31 and the second main switch 33 are ON (the switching circuit 30 is ON), the input DC voltage E_i is applied to the inductor 2, and magnetic energy is stored.

When the rising oscillation voltage V_t and

the error voltage V_{e1} intersect with each other at time t_1 , the signal V_1 and the drive signal V_{g31} become low, whereby the first main switch 31 becomes OFF. At this time, the magnetic energy stored in the inductor 2 is released as a current for charging the capacitor 51 via the diode 41 since the auxiliary switch 32 is OFF (the switching circuit 30A is in its first OFF state). Hence, the current flowing through the inductor 2 decreases and becomes zero soon.

At time t_2 , both the frequency-divided signal V_{t2} and the frequency-divided signal V_{t3} are driven high by the clock signal V_{t1} , whereby the oscillation voltage V_t lowers abruptly and then starts rising. The output of the AND gate 151, that is, the signal V_{32} , becomes high, and the drive signal V_{g32} also becomes high, whereby the auxiliary switch 32 becomes ON. The AND gate 152 outputs the signal V_2 , and both the outputs of the AND gates 153 and 154 become low, whereby the signal V_2 is output as the signal V_{31} via the OR gate 155. In other words, the signal V_2 obtained as the result of the comparison between the oscillation voltage V_t and the error voltage V_{e2} is selected as the drive signal V_{g31} . Since the signal V_2 , that is, the drive signal V_{g31} , is high, the first main switch 31 becomes ON. In addition, since the output of the OR gate 156, that is,

the signal V33, is high, the drive signal Vg33 also becomes high, and the second main switch 33 becomes ON. Since the switching circuit 30A becomes ON at this time, the input DC voltage Ei is applied to the inductor 2, and magnetic energy is stored.

When the rising oscillation voltage Vt and the error voltage Ve2 intersect with each other at time t3, the signal V2 and the drive signal Vg31 become low, whereby the first main switch 31 becomes OFF. At this time, the magnetic energy stored in the inductor 2 is released as a current for charging the capacitor 52 via the diode 42 since the auxiliary switch 32 is ON (the switching circuit 30A is in its second OFF state). Hence, the current flowing through the inductor 2 decreases and becomes zero soon.

At time t4, the frequency-divided signal Vt2 is driven low by the clock signal Vt1, but the frequency-divided signal Vt3 remains low. The oscillation voltage Vt lowers abruptly and then starts rising again. Since the output of the AND gate 151 is low, the drive signal Vg32 also becomes low, and the auxiliary switch 32 becomes OFF. Both the outputs of the AND gates 152 and 153 are low, whereby the signal V1 output from the AND gate 154 is output as the signal V31. In other words, the signal V1 is selected as the drive signal Vg31. Since the signal V1, that

is, the drive signal V_{g31} , is high, the first main switch 31 becomes ON. In addition, since the output of the OR gate 156, that is, the signal V_{33} , is high, the drive signal V_{g33} also becomes high, and the second main switch 33 becomes ON. Since the first main switch 31 and the second main switch 33 are ON (the switching circuit 30A is ON), the input DC voltage E_i is applied to the inductor 2, and magnetic energy is stored.

At time t_5 , the signal V_1 and the drive signal V_{g31} become low, whereby the first main switch 31 becomes OFF. Since the auxiliary switch 32 is OFF (the switching circuit 30A is in its first OFF state) at this time, the current flowing through the inductor 2 charges the capacitor 51 via the diode 41. The current flowing through the inductor 2 then decreases and becomes zero soon. The operations at time t_4 and time t_5 are similar to those at time t_0 and time t_1 , respectively.

At time t_6 , the frequency-divided signal V_{t2} is driven high and the frequency-divided signal V_{t3} is driven low by the clock signal V_{t1} , whereby the oscillation voltage V_t lowers abruptly and then starts rising. The output of the AND gate 151, that is, the signal V_{32} , becomes low, and the drive signal V_{g32} also becomes low, whereby the auxiliary switch 32

becomes OFF. Both the outputs of the AND gates 152 and 154 are low, but the output of the AND gate 153 is high. Hence, the signal V31 output via the OR gate 155, that is, the drive signal Vg31, becomes high, and the first main switch 31 becomes ON. In addition, the signal V3 is selected as the output of the OR gate 156, that is, the signal V33. The signal V3, that is, the drive signal Vg33, also becomes high, and the second main switch 33 becomes ON. Since the switching circuit 30A becomes ON, the input DC voltage E_i is applied to the inductor 2, and magnetic energy is stored.

When the rising oscillation voltage V_t and the error voltage V_{e3} intersect with each other at time t_7 , the signal V3 and the drive signal Vg33 become low, whereby the second main switch 33 becomes OFF. At this time, the magnetic energy stored in the inductor 2 is released as a current for charging the capacitor 53 via the diode 43 since the first main switch 31 is ON (the switching circuit 30A is in its third OFF state). Hence, the current flowing through the inductor 2 decreases and becomes zero soon.

At time t_8 , the frequency-divided signal V_{t2} is driven low by the clock signal V_{t1} , but the frequency-divided signal V_{t3} remains low. The switching circuit 30A becomes ON again. After time t_8 ,

the operation at time t_0 and thereafter is repeated.

It is assumed that the inductance of the inductor 2 is L , that the switching cycle is T , that the ON period of the switching circuit 30A before its first OFF state is T_{on1} , that the ON period of the switching circuit 30A before its second OFF state is T_{on2} , and that the ON period of the switching circuit 30A before its third OFF state is T_{on3} . In addition, it is assumed that the output current to the first load 6 is I_{o1} , that the output current to the second load 10 is I_{o2} , and that the output current to the third load 63 is I_{o3} . Furthermore it is assumed that the forward voltage drops of the diodes 41, 42 and 43 are neglected. On the basis of these assumptions, the first output voltage V_{o1} , the second output voltage V_{o2} and the third output voltage V_{o3} are represented by the following equations (7), (8) and (9), respectively.

$$V_{o1} = E_i + \frac{(E_i \cdot T_{on1})^2}{4L \cdot T \cdot I_{o1}} \quad (7)$$

$$V_{o2} = E_i + \frac{(E_i \cdot T_{on2})^2}{8L \cdot T \cdot I_{o2}} \quad (8)$$

$$V_{o3} = - \frac{(E_i \cdot T_{on3})^2}{8L \cdot T \cdot I_{o3}} \quad (9)$$

In the multi-output DC-DC converter in accordance with Embodiment 3, the error voltages V_{e1} , V_{e2} and V_{e3} change so that the first, second and third output voltages V_{o1} , V_{o2} and V_{o3} are stabilized to their respective desired voltages, whereby each ON period of the switching circuit 30A is adjusted. In other words, in the multi-output DC-DC converter in accordance with Embodiment 3, the two boost converters and the one buck-boost converter, in which the inductor 2 is commonly used, are subjected to time-sharing control. Hence, the first, second and third output voltages V_{o1} , V_{o2} and V_{o3} are stabilized to their respective desired voltages. In the above-mentioned Embodiment 3, a case wherein a half of the switching frequency is assigned to the control of the first output voltage V_{o1} , a quarter of the switching frequency is assigned to the control of the second output voltage V_{o2} , and a quarter of the switching frequency is assigned to the control of the third output voltage V_{o3} is taken as an example. In the multi-output DC-DC converter in accordance with the present invention, the switching frequencies to be assigned to the control of the respective output

voltages are determined so as to have appropriate ratios.

FIG. 7B shows the state of the drive signal Vg31 obtained by the OR gates 161 and 162 and the AND gate 163, the state of the drive signal Vg32 obtained by the OR gates 164 and the AND gate 165, and the state of the drive signal Vg33 obtained by the OR gates 166 and 168 and the AND gate 167, depending on the high and low states of the signals Vx1, Vx2 and Vx3.

State I(1) in FIG. 7B corresponds to the normal operation condition wherein all the signals Vx1, Vx2 and Vx3 are high. In addition, state VIII(8) is the abnormal condition wherein all the signals Vx1, Vx2 and Vx3 are low. In this case, the output of the NOR gate 118 becomes high, and the shutdown circuit 119 is activated.

At the time of starting or overload, the operation in the case when one of the output voltages is in an overvoltage condition, shown in states II(2) to VII(7), will be described below.

States II(2) to IV(4) in FIG. 7B correspond to a case wherein the first load 6 is increased and the first output current Iol is in an overcurrent condition, for example. In this case, a phenomenon occurs wherein the current flowing through the

inductor 2 does not become zero within the switching cycle assigned to the control of the first output voltage V_{o1} .

The magnetic energy not released but remaining in the inductor 2 is released as a current for charging the capacitor 53 in the third OFF state (the first main switch 31 is ON, the auxiliary switch 32 is OFF, and the second main switch 33 is OFF) in the next switching cycle. If the average value of this release current is larger than the current consumed by the third load 63, the third output voltage V_{o3} gets into an overvoltage condition, and the signal V_{x3} become low. State II(2) corresponds to the above-mentioned condition wherein the signals V_{x1} and V_{x2} are high and the signal V_{x3} is low. At this time, the drive signal V_{g31} become low, and the drive signal V_{g32} becomes the signal V_{32} . However, since the third OFF state continues, the drive signal V_{g32} becomes low in the circuit configuration of Embodiment 3. Then, the drive signal V_{g33} becomes high, and the switching circuit 30A gets into its first OFF state (the first main switch 31 is OFF, the auxiliary switch 32 is OFF, and the second main switch is ON). Hence, the release of the magnetic energy of the inductor 2 is shifted from the third output to the first output, whereby the overvoltage condition of the third output

voltage V_{o3} is avoided.

In the case of state III(3), the magnetic energy not released but remaining in the inductor 2 is released as a current for charging the capacitor 52 in the second OFF state (the first main switch 31 is OFF, the second main switch 33 is ON, and the auxiliary switch 32 is ON) in the next switching cycle. If the average value of this release current is larger than the current consumed by the second load 10, the second output voltage V_{o2} gets into an overvoltage condition, and the signal V_{x2} become low. At this time, the drive signal V_{g31} is the signal V_{31} . However, since the second OFF state continues, the drive signal V_{g31} becomes low. The drive signal V_{g32} becomes low, and the drive signal V_{g33} becomes the signal V_{33} . However, since the second OFF state continues, the drive signal V_{g33} becomes high. In other words, the switching circuit 30A gets into its first OFF state. Hence, the release of the magnetic energy of the inductor 2 is shifted from the second output to the first output, whereby the overvoltage condition of the second output voltage V_{o2} is avoided.

In the case of state IV(4), both the second output voltage V_{o2} and the third output voltage V_{o3} get into overvoltage conditions, and the signals V_{x2} and V_{x3} become low. At this time, the drive signal

Vg31 becomes low, the drive signal Vg32 becomes low, and the drive signal Vg33 becomes high. In other words, the switching circuit 30A gets into its first OFF state. The release of the magnetic energy of the inductor 2 is shifted to the first output, whereby the overvoltage conditions of the second output voltage Vo2 and the third output voltage Vo3 are avoided.

Next, in the case of state V(5), the second output current Io2 or the third output current Io3 is in an overcurrent condition, for example. In this case, a phenomenon occurs wherein the current flowing through the inductor 2 does not become zero within the switching cycle assigned to the control of the second output voltage Vo2 or the third output voltage Vo3. The magnetic energy not released but remaining in the inductor 2 is released as a current for charging the capacitor 51 in the first OFF state in the next switching cycle. If the average value of this release current is larger than the current consumed by the first load 6, the first output voltage Vo1 gets into an overvoltage condition, and the signal Vx1 become low. At this time, the drive signal Vg31 is the signal V31. However, since the first OFF state continues, the drive signal Vg31 becomes low. The drive signal Vg33 becomes the signal V33. However, since the first OFF state continues, the drive signal

Vg33 becomes high. Furthermore, the drive signal Vg32 becomes high. As a result, the switching circuit 30A gets into its second OFF state. The release of the magnetic energy of the inductor 2 is shifted from the first output to the second output, whereby the overvoltage condition of the first output voltage Vol is avoided.

In the case of state VI(6), the second output current Io2 is in an overcurrent condition and the other output currents are very small, for example. The magnetic energy not released but remaining in the inductor 2 within the switching cycle assigned to the control of the second output voltage Vo2 raises the first output voltage Vol to an overvoltage condition in the first OFF state in the next switching cycle. In addition, in the third OFF state in the next switching cycle, the third output voltage Vo3 is raised to an overvoltage condition. Furthermore, the signals Vx1 and Vx3 become low. At this time, the drive signal Vg31 becomes low, the drive signal Vg32 becomes high, and the drive signal Vg33 becomes high. In other words, the switching circuit 30A gets into its second OFF state. The release of the magnetic energy of the inductor 2 is shifted to the second output, whereby the overvoltage conditions of the first output voltage Vol and the overvoltage condition

of the third output voltage V_{o3} are avoided.

In the case of state VII(7), the third output current I_{o3} is in an overcurrent condition and the other output currents are very small, for example. The magnetic energy not released but remaining in the inductor 2 within the switching cycle assigned to the control of the third output voltage V_{o3} raises the first output voltage V_{o1} to an overvoltage condition in the first OFF state in the next switching cycle. In addition, in the second OFF state in the next switching cycle, the second output voltage V_{o2} is raised to an overvoltage condition. Furthermore, the signals V_{x1} and V_{x2} become low. At this time, the drive signal V_{g31} becomes high, the drive signal V_{g32} becomes low, and the drive signal V_{g33} becomes low. In other words, the switching circuit 30A gets into its third OFF state. The release of the magnetic energy of the inductor 2 is shifted to the third output, whereby the overvoltage conditions of the first output voltage V_{o1} and the overvoltage condition of the second output voltage V_{o2} are avoided.

As described above, in the above-mentioned Embodiment 3 in accordance with the present invention, even if the current flowing through the inductor 2 does not become zero within one switching cycle and the output voltage rises and becomes uncontrollable at

the time of starting or overload, the overvoltage condition is detected, and the magnetic energy remaining in the inductor 2 is released to the other output. Hence, the overvoltage condition can be avoided.

As made obvious from the detailed explanations of the embodiments, the present invention has the following effects.

The multi-output DC-DC converter in accordance with the present invention comprising a plurality of converters, wherein the main switch and the inductor are commonly used so that the number of components is reduced, has an excellent effect capable of controlling any of a plurality of outputs at high efficiency.

In addition, even in the case of the abnormal condition, for example, at the time of starting or overload, the multi-output DC-DC converter in accordance with the present invention is configured so that the operation shifts to the next cycle after the current flowing through the inductor becomes zero within one switching cycle, as described in the explanations of Embodiment 1, for example. Hence, it is possible to avoid an overvoltage condition due to the occurrence that the current flowing through the inductor does not become zero within one switching

cycle.

Furthermore, the multi-output DC-DC converter in accordance with the present invention is configured as described below. For example, as described in the explanations of Embodiments 2 and 3, the current flowing through the inductor does not become zero within one switching cycle occurs in some cases since the switching cycle is fixed. However, the resulting overvoltage condition is detected, and the current is released to the other output. Therefore, the multi-output DC-DC converter has an excellent effect capable of avoiding the overvoltage condition.

Although the present invention has been described with respect to its preferred embodiments in sine detail, the disclosed contents of the preferred embodiments may change in the details of the structure thereof, and any changes in the combination and sequence of the components may be attained without departing from the spirit and scope of the claimed invention.